REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 3-17 and 20-29 are pending in the present application. Claims 1, 3, 4, 10, 12, 16, 17, 20, 26 and 27 have been amended and claims 2, 18 and 19 have been canceled by the present amendment.

In the outstanding Office Action, claims 2-15 and 18-29 were rejected under 35 U.S.C. § 112, first paragraph; claims 1 and 12 were rejected under 35 U.S.C. § 102(e) as anticipated by Taylor et al.; and claims 1, 16 and 17 were rejected under 35 U.S.C. § 102(e) as anticipated by Nguyen et al.

Claims 2-15 and 18-29 stand rejected under 35 U.S.C. § 112, first paragraph. This rejection is respectfully traversed.

The Office Action indicates the limitations in claims 2, 12, 18 and 26 have not been enabled in the specification. It is respectfully noted the subject matter originally cited in claim 2 has been amended and incorporated into independent claim 1. In particular, independent claim 1 now recites that the multi clock deciding system includes a plurality of slave clock deciding apparatuses (slaves) and a multi clock selecting unit configured to receive the clock signals of the master and slaves and to supply the system clock signal to the master and slaves. These features are shown in a non-limiting example in Figure 7, for example.

In particular, Figure 7 illustrates a multi clock selecting unit 710 configured to receive clock signals for the master and slaves (i.e., clock signal 1, clock signal 2, clock signal 3 ... clock signal N) and to supply the system clock signal output by the selecting unit 710 to the master and slaves. Note that assuming the first clock decoding apparatus is a master and the other apparatuses are slaves, the clock signal 1 in this example would be the system clock. The other signals 2, 3 ... N would be a clock signal selected from the plurality of delay clock signals having a minimum phase difference from the system clock. The multi clock selecting unit 710 then receives the clock signals 1, 2, 3 ... N from the master and slaves, and outputs one of these signals as the system clock. Note dependent claim 3 further defines that the selecting unit outputs one of the slave clock signals if there is an error on the master clock signal (e.g., in the above example, the selecting unit 710 would select a clock signal from clock signals 2, 3 ... N if there was an error in the clock signal 1). These features are also described in the specification at paragraphs [43-45], for example.

In addition, the features recited in dependent claim 12 are illustrated in a non-limiting example in Figure 2, for example. In more detail, Figure 2 illustrates a slave clock deciding apparatus in which a reference clock signal input into the PLL circuit 200 is converted into the frequency used in the system (the P-REF SIGNAL). Then, the slave generates the plurality of delay clock signals by delaying the converted frequency clock signal for a predetermined time. The phase comparing unit 220 compares a phase of the system clock signal (the outer clock signal) to phases of the respective delay clock signals. The clock

selecting unit 250 selects and outputs one of the delay clock signals having a minimum phase difference from the system clock signal by referring to the phase comparison result. These features are also described in the specification at paragraphs [25-29], for example. Similar comments apply to dependent claim 26.

In addition, claim 18 has been canceled and some of the subject matter recited therein has been incorporated into independent claim 17. In particular, independent claim 17 is directed to a multi clock selecting method, which includes receiving the output clock signals in a selecting unit, and supplying a system clock signal from the selecting unit to respective clock devices that generate the first and second output signals. Further, the selecting unit outputs the second output clock signal as the system clock signal if there is an error in the first output clock signal. These features are also shown in the non-limiting example of Figure 7, for example, and are described in the specification at page 12, paragraph [44], for example.

Accordingly, in light of the above comments, it is respectfully submitted claims 2, 12, 18 and 26 are enabled by the specification and therefore it is requested this rejection be withdrawn.

As noted above, independent claim 1 has been amended to include subject matter similar to that recited in dependent claim 2, and independent claim 17 has been amended to include some of subject matter similar to that recited in dependent claims 18 and 19. Accordingly, the rejection of claims 1 and 12 under 35 U.S.C. § 102(e) as anticipated by

Taylor et al. and the rejection of claims 1 and 17 under 35 U.S.C. § 102(e) as anticipated by Nguyen et al. are moot.

Further, dependent claim 16 has been rewritten into independent form. In particular, claim 16 recites that the output of the master is directly inputted into the slave and the output of the slave is directly inputted into the master. These features are shown in a non-limiting example in Figure 6, for example, in which it is assumed the clock deciding apparatus 600a is the master and the clock deciding 600b is the slave. As shown, the novel structure of the present invention includes the master clock deciding apparatus 600a and the slave clock deciding apparatus 600b configured to generate a plurality of delay clock signals by delaying a reference clock signal, and to output a clock signal selected from the plurality of delay clock signals having a minimum phase difference from the system clock. Further, the output of the master 600a is directly inputted into the slave 600b and the output of the slave 600b is directly inputted into the master 600a. See also the corresponding description in the specification regarding Figure 6.

On the contrary, Nguyen et al. does not teach or suggest the claimed configuration. That is, Nguyen does not teach or suggest an output of a master being directly input into a slave and the output of the slave being directly input into the master as claimed by the present invention. Taylor et al. also does not teach or suggest these features.

Accordingly, it is respectfully submitted independent claim 16 is also allowable.

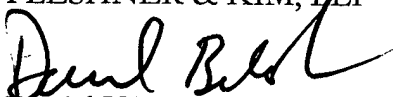
Further, the specification has been amended to correct minor informalities. No new matter has been added.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, **David A. Bilodeau**, at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



Daniel Y.J. Kim, Esq.
Registration No. 36,186
David A. Bilodeau, Esq.
Registration No. 42,325

P.O. Box 221200
Chantilly, Virginia 20153-1200
703 766-3701 DYK/DAB:cre:lew
Date: December 20, 2004

Please direct all correspondence to Customer Number 34610